ZC0301

VGA USB PC Camera Controller

Vimicro Corporation

Preliminary

Data Sheet

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Illustrations

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1. Features

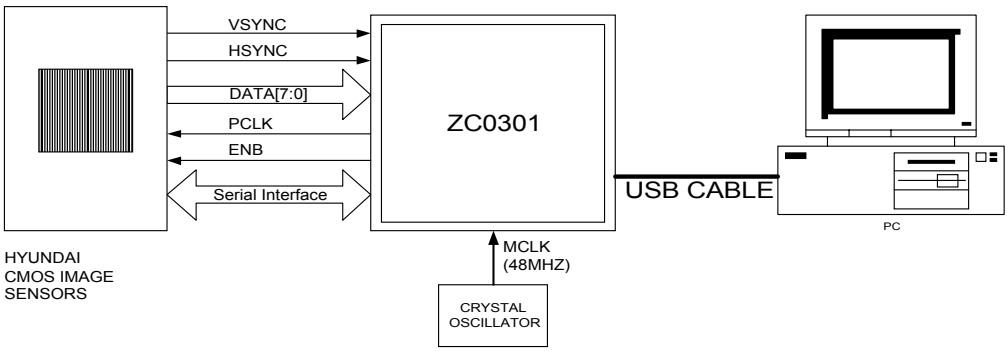


Figure 1 USB PC Camera System Block Diagram

With a miniature 28-Pin PLCC package and without external DRAM, ZC0301 provides a cost effective single chip solution for PC camera application. All major image processing functions, image data compression, and data transfer units are built in the chip. The ZC0301 chip communicates with PC host via Universal Serial Bus (USB) port.

- Provide most cost effective PC camera solution with 28-pin package
- Support VGA CMOS sensors from Hyundai
- Support up to 15 fps VGA video display without DRAM
- USB Device Controller compliant with USB Protocol 1.1
- Support pan function based on 8x8 pixels unit
- Support 8-bit RGB Bayer pattern raw data input from CMOS image sensors
- Support 2-wire control interface to CMOS image sensor
- Support programmable color correction and gamma correction
- Support AE/AWB and programmable AE/AWB windows
- Support automatic CMOS sensor Reset Level Control
- Support automatic Gain Control
- Support auto/manual Histogram Equalization
- Support 2x2 Sub-Sampling
- Support ISO/IEC 10918-1 (JPEG) standard image compression
- Support JPEG File Interchange Format (JFIF) compressed image data output
- Support 2 AC and 2 DC Huffman code table
- Support 4 quantization tables for programmable image quality
- Adjustable compression ratio
- Support Custom-ID option

2. Architecture

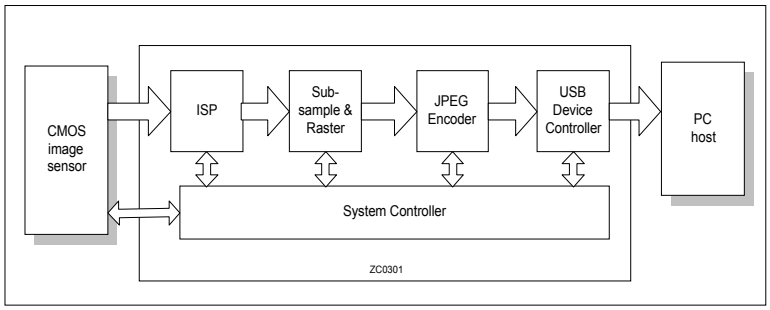


Figure 2 ZC0301 Functional Block Diagram

The ZC0301 consists of five major function blocks, *System Controller, Image Signal Processor, Sub-Sample & Raster, JPEG Encoder,* and *USB Device Controller,* as illustrated in Figure 1. These blocks provide the following functions.

2.1. System Controller

- Providing the control to ISP, JPEG, and USB blocks
- Configuring the control registers
- Chip clock generation
- Error control for the data block through USB interface

2.2. Image Signal Processor

- Dedicated sensor control and signal processing module.
- Serial-Bus interface for CMOS Image Sensor
- 8 bit Bayer format image input
- 3x3 Interpolation
- Color Correction
- Gamma Correction
- Automatic Exposure Control
- Automatic White Balance Control
- Programmable AE windows
- Automatic Reset Level Control
- RGB to YCrCb Color Space Convert
- Histogram Equalization Logic

2.3. Sub-Sample & Raster

- The input data format is 4:4:4 for Y component, Cb component and Cr component. The three components for a pixel are input simultaneously.

- The output data format is in 4:2:2 for the three components. The output sequence is Y,Y,Cb,Cr for the three components.
- When scale option is deserted, the output pixel number is the same as the input pixel number; when scale option is asserted, the output pixel number is 1/4 of the pixel number of input image.
- Change input image data format to 8x8 block data format required by DCT module.

2.4. JPEG Encoder

- Providing register control for image size, compression rate and the image quantity.
- Compliant with ISO/IEC 10918-1 standard.

2.5. USB Device Controller

- Compliant with USB protocol 1.1
- Support full speed USB device
- Clock and data recovery from USB
- Bit stripping/stuffing and NRZI decoder/encoder
- Check all possible error conditions, including CRC error, bit stuffing error, PID error, as well as synchronization error
- Support all standard request and vendor/class request
- Configuration can be changed easily to support different applications
- Support suspend mode

3. Pin Definition

3.1. Pin Assignment

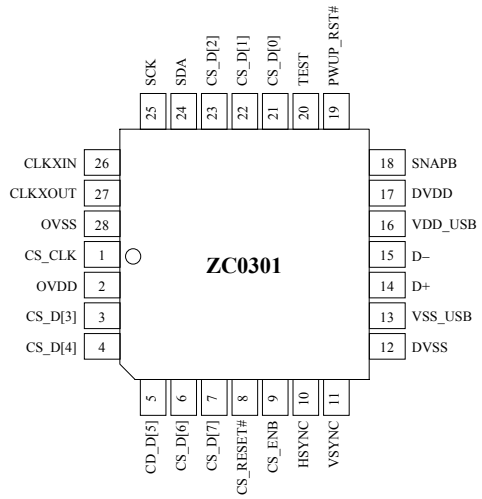


Figure 3 28-Pin PLCC Package

3.2. Pin Description

Table 1 Sensor Interface (15 Pins)

Signal	Function	Type	28 PLCC Pin #
CS_D[5]	Sensor data	I/O, PD	5
CS_D[6]	Sensor data	I, PD	6
CS_D[7]	Sensor data	I, PD	7
CS_RESET#	Sensor reset	O	8
CS_ENB	Sensor power enable	I/O	9
HSYNC	Horizontal sync	I, PD	10
VSYNC	Vertical sync	I, PD	11
CS_D[0]	Sensor data	I, PD	21
CS_D[1]	Sensor data	I, PD	22
CS_D[2]	Sensor data	I, PD	23
SDA/ESDA	IIC/EEPROM data	I/O, Schmitt	24

SCK/ESCK	IIC/EEPROM clock	O	25
CS_CLK	Sensor clock	O	1
CS_D[3]	Sensor data	I/O, PD	3
CS_D[4]	Sensor data	I/O, PD	4

Table 2 USB Host Interface (2 Pins)

Signal	Function	Type	28 PLCC Pin #
D+	USB data	I/O	14
D–	USB data	I/O	15

Table 3 Clock, Reset, and Miscellaneous (5 Pins)

Signal	Function	Type	28 PLCC Pin #
SNAPB	Snap, scan in	I, PU	18
PWUP_RST#	Power-on reset	I, Schmitt	19
TEST	Manufacturing test enable, Tied to GND on board	I, PD	20
CLKXIN	Crystal input	I	26
CLKXOUT	Crystal output	O	27

Table 4 Power and Ground (6 Pins)

Signal	Function	Type	28 PLCC Pin #
DVSS	Core ground	P	12
VSS_USB	USB transceiver ground	P	13
VDD_USB	USB transceiver power	P	16
DVDD	Core power (2.5V)	P	17
OVSS	I/O ground	P	28
OVDD	I/O power (3.3V)	P	2

4. Electrical Characteristics

4.1. Absolute Maximum Ratings

Table 5 Maximum Ratings

Ambient temperature	0°C to 70°C
Storage temperature	-40°C to 125°C
DC supply voltage	-0.3V to 3.6V
I/O pin voltage with respect to VSS	-0.3V to VDD + 0.3V

4.2. DC Characteristics

Table 6 DC Characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
VDD3V	3.3V Power Supply		3.0	3.6	V
VDD2V	2.5V Power Supply		2.25	2.75	V
Vil	Input Low voltage		-0.5	1.0	V
Vih	Input High voltage		2.3	5.5	V
Vol	Output Low Voltage		-	0.4	V
Voh	Output High Voltage		2.4	-	V
Ipd	Powerdown current (suspend current)		-	500	uA
Ido	Active current		-	60	mA

4.3. USB Transceiver AC Characteristics

Table 7 Full-Speed Driver Electrical Characteristics

Symbol	Parameter	Conditions	Min Typ Max	Unit
T_{FR}	Rise time	C_L=50p	4 20	ns
T_{FF}	Fall time	C_L=50p	4 20	ns
T_{FRFF}	Rise and fall time matching	$T_{LRLF}=T_{LR}/T_{LF}$	90 111.11	%

Table 8 Low-Speed Driver Electrical Characteristics

Symbol	Parameter	Conditions	Min Typ Max	Unit
T_{LR}	Rise time	C_L=50p C_L=600p	75 300	ns
T_{LF}	Fall time	C_L=50p C_L=600p	75 300	ns
T_{LRLF}	Rise and fall time matching	$T_{LRLF}=T_{LR}/T_{LF}$	80 125	%

4.4. RESET Timing AC Characteristics

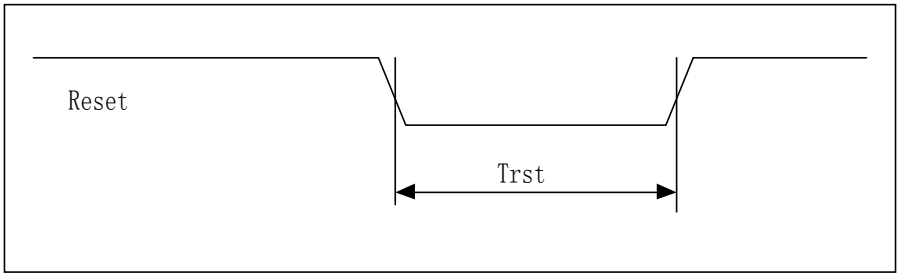


Figure 4 RESET Timing AC Characteristics Diagram

Table 9 Reset Signal AC Characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
Trst	Reset Pulse Width		100	-	ms

4.5. Clock AC Characteristics

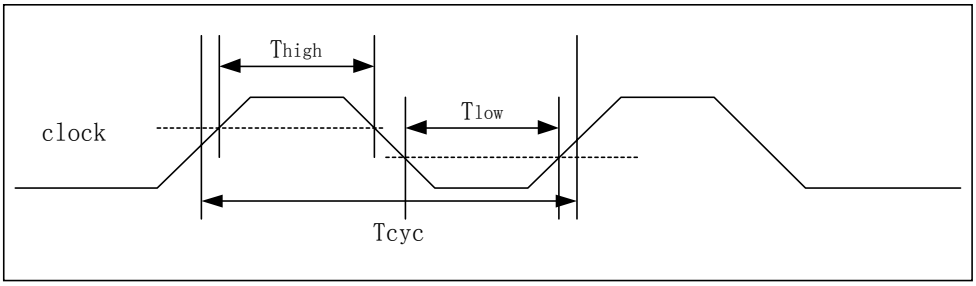


Figure 5 Clock Timing AC Characteristics Diagram

Table 10 Clock Signal AC Characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
1/Tcyc	Oscillator Frequency	48@10PPM	-	-	Mhz
Thigh	Oscillator Clock High Time		8.3	-	Ns
Tlow	Oscillator Clock Low Time		8.3	-	Ns

4.6. Input Signal AC Characteristics

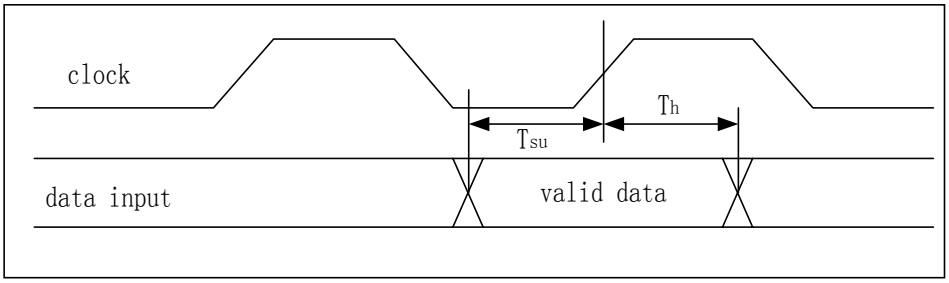


Figure 6 Input Signal Timing AC Characteristics Diagrams

Table 11 Input Signal AC Characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
T_{su}	Input setup time		18	-	ns
T_h	Input hold time		0	-	ns

5. Register Table (Vendor Commands)

Table 12 System Control Register

Address	Symbol	Register Name	Default	Access
0180H	SysCon	System control register	00H	R/W
0181H	SysOp	System enable register	00H	R/W
0183H	ImWidthH	Image width high byte	02H	R/W
0184H	ImWidthL	Image width low byte	80H	R/W
0185H	ImHeightH	Image height high byte	01H	R/W
0186H	ImHeightL	Image height low byte	E0H	R/W
0187H	TbrcReg	JPEG BRC register	00H	R/W
0188H	QuanReg	JPEG Quantization register	00H	R/W
0189H	LEVEL1_ADDR	Target image size for state 1	40H	R/W
018AH	LEVEL2_ADDR	Target image size for state 2	60H	R/W
018BH	LEVEL3_ADDR	Target image size for state 3	80H	R/W
018DH	CustomID	Custom ID		RO
018EH	FrameConEn	Frame Control Enable	01H	R/W
018FH	Frame State	Frame Control State		RO
0190H	LEVEL1Data_add	Hblank value for state 1	0AH	R/W
0191H	LEVEL2Data_add	Hblank value for state 2	1BH	R/W
0192H	LEVEL3Data_add	Hblank value for state 3	3CH	R/W

6. Mechanical Information

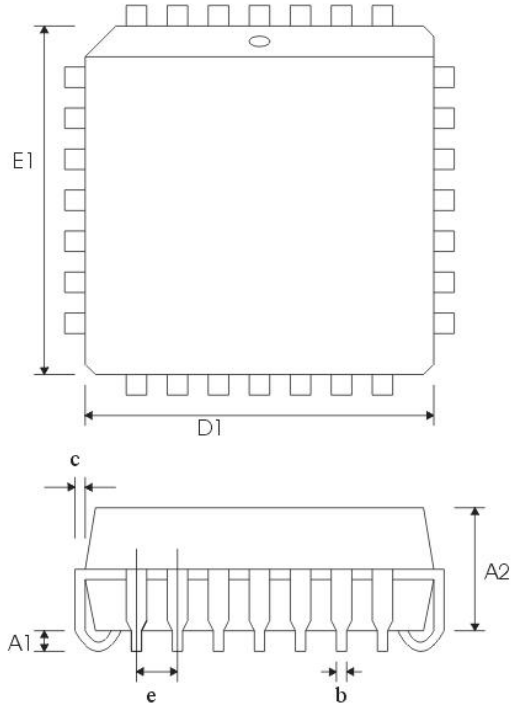


Figure 7 28-Pin PLCC Package Diagram

Table 13 ZC0301 Package Dimension

Lead Count		28
Body Size	D1	453
	E1	453
Stand-Off	A1	20
Body Thickness	A2	150
Lead Width	b	17
Lead Thickness	c	10
Lead Pitch	e	50

Unit: mil (1mil = 1/1000 inch)

Appendix I Sensor Interface Description

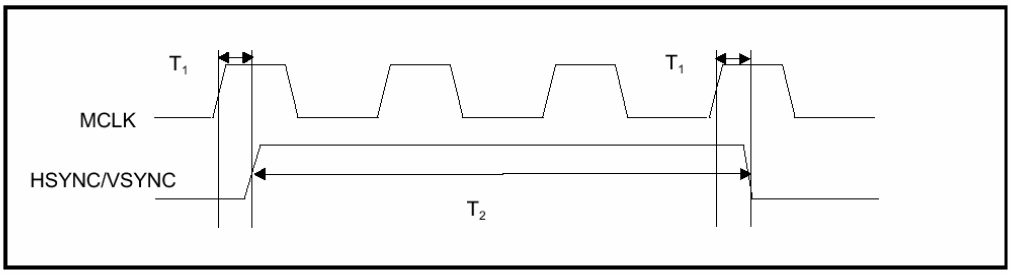
ZC0301 supports Hyundai VGA format sensors (HV7131B).

1. INPUT / OUTPUT AC CHARACTERISTICS

All output timing delays are measured with output load 60pF
Output delay includes the internal clock path delay [6ns] and output driving delay that changes in respect to the output load, the operating environments, and a board design.
Due to the variable valid time delay of the output, output signals may be latched in the negative edge of MCLK for the stable data transfer between the image sensor and a host for less than 15MHz operation.

2. MCLK TO HSYNC / VSYNC Timing

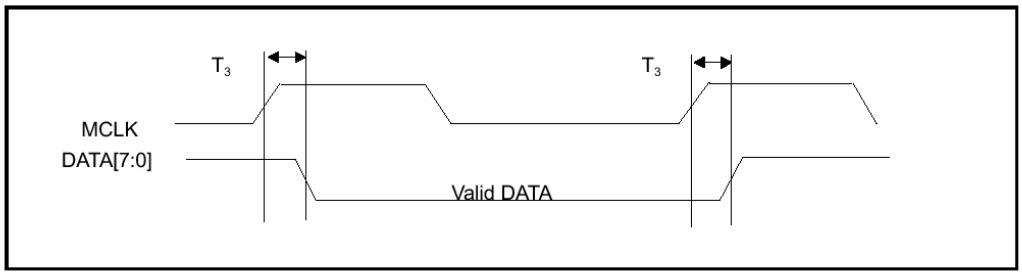
FIGURE 8.1-1 MCLK TO HSYNC/VSYNC TIMING DIAGRAM



T1: MCLK RISING TO HSYNC/VSYNC valid maximum Time: 18ns [output load: 60pF]
T2: HSYNC/VSYNC valid Time: minimum 1 clock (subject to T1, T2 timing rule)

3. MCLK to DATA Timing

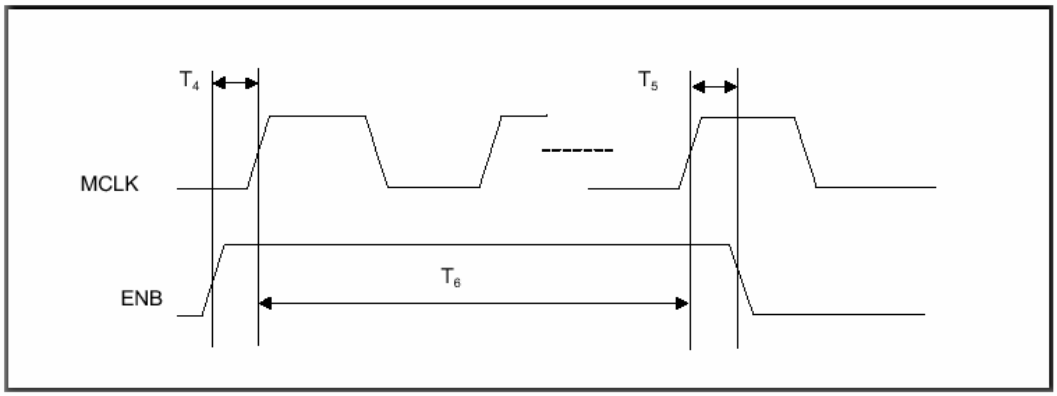
FIGURE 8.1-2 MCLK TO DATATIMING DIAGRAM



T3: MCLK rising to DATA Valid maximum Time: 18ns [output load:60pF]
Note: HSYNC signal is high when valid data is on the DATA bus.

4. ENB Timing

FIGURE 8.1-3 ENB TIMING DIAGRAM



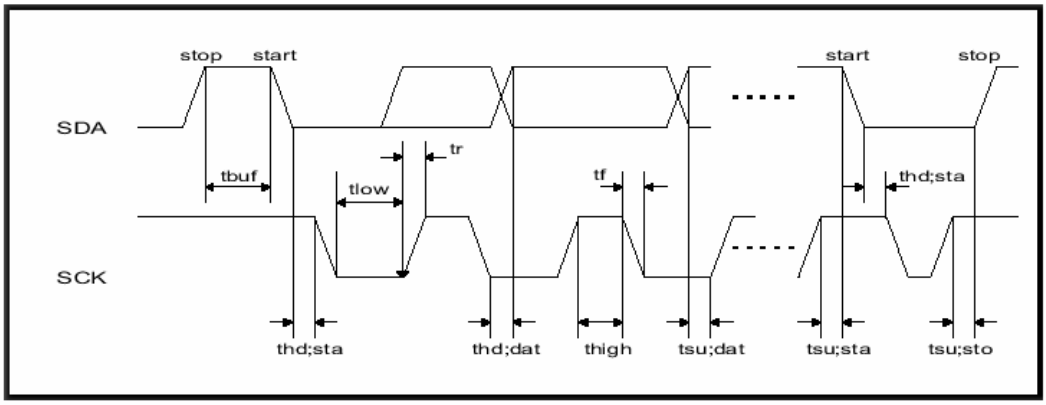
T4: ENB Setup Time: 5[ns]
T5: ENB Hold Time: 5[ns]
T6: ENB Valid Time: minimum 2 Clock

5. RESET Timing

Must in Valid (active low) state at least 8 MCLK periods

6. I²C Bus (Programming Serial Bus) Timing

FIGURE 8.1-4 I²C BUS TIMING DIAGRAM



7. I²C Bus Interface Timing

Parameter	Symbol	Min	Max.	Unit
SCK clock frequency	f_{sck}	0	400	KHz
Time that I²C bus must be free before a new transmission can start	t_{buf}	1.2	-	Us
Hold time for a START	$t_{hd};S_{ta}$	1.0	-	Us
LOW period of SCK	t_{low}	1.2	-	Us
HIGH period of SCK	t_{high}	1.0	-	Us
Setup time for START	$t_{su};S_{ta}$	1.2	-	Us
Data hold time	$t_{hd};d_{at}$	1.3	-	Us

Data setup time	$t_{su};d_{at}$	250	-	Ns
Rise time of both SDA and SCK	t_r	-	250	Ns
Fall time of both SDA and SCK	t_f	-	300	Ns
Setup time for STOP	$t_{su};S_{tp}$	1.2	-	Us
Capacitive load of each bus lines (SDA, SCK)	C_b	-	-	Pf

Table 8.1 I^2C Bus Interface Timing

8. Connection for HV7131B

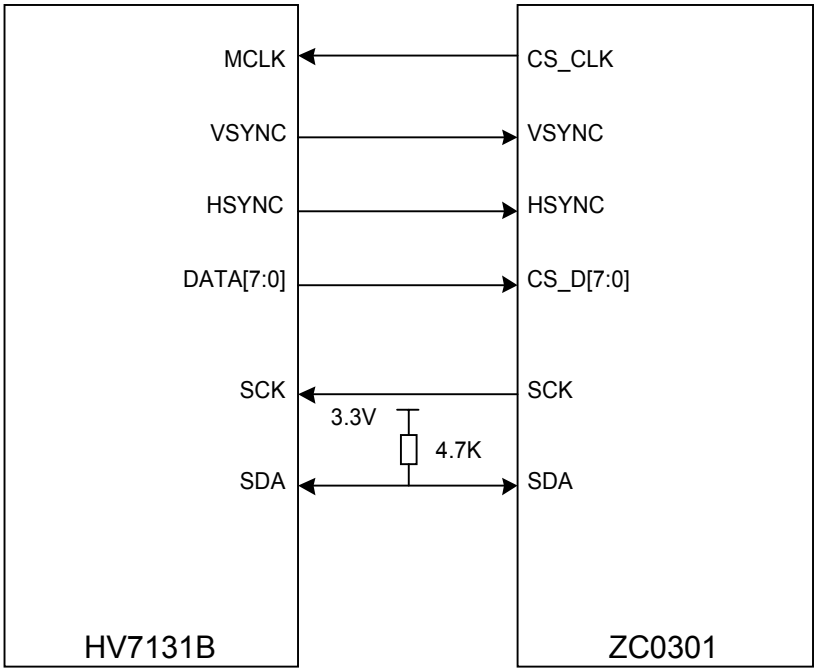


FIGURE 8.1-5 PERIPHERAL CONNECTION DIAGRAM

Note:
1. For Hyundai sensor, RESETB is active LOW.